ABSTRACT OF THE DISCLOSURE

A method is provided for manufacturing an integrated circuit device having a plurality of wiring layers including a first wiring layer which is not the upper most layer among the plurality of wiring layers and a second wiring layer higher than the first wiring layer in the plurality of wiring layers. An interlayer dielectric film is provided to cover the first wiring layer. Holes are then formed in the interlayer dielectric film and a mask film is formed to cover some of the holes. Etching using the mask film is then carried out and an insulating film formed on the interlayer dielectric film is removed, including the bottoms and/or insides of the holes. The mask film is then removed and a conductive member is formed inside the holes.